**Digital Design (CSCE 2114) – Lab 7**

In this lab you are to write VHDL code to implement a rising edge triggered T flip-flop that has an asynchronous active low clear input and an asynchronous active low preset input. If both the clear and preset are asserted then the flip flop is cleared.

The signal names are to be:

Clk – clock input (rising edge triggered)

T – T (toggle) input

Pren – active low asynchronous preset

Clrn – active low asynchronous clear

Q – Q output of flip-flop

Qn – Qn output of flip-flop (invert of Q)

Steps:

1. Create a new project and VHDL file. It’s best not to use the default project directory that Quartus lists. Name the project file, VHDL file, and entities (in the code) the same name.
2. After finishing your code, compile your project and correct any errors.
3. Create a waveform file to apply the test patterns shown in the figure below. Run the simulation and check the outputs. The order of the inputs and outputs in the waveform should be Clk, T, Pren, Clrn, Q, then Qn.
4. Remember to save your results (waveforms) and explain them in your lab report.

Report

Save and print out the VHDL and waveforms. Describe each condition that was tested to show correct functionality.



**Testing waveforms**